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	Search Text
1	"20020126029"
2	(grale near3 (trenton john)) or (chen near3 sijian)
3	(delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2
4	((grale near3 (trenton john)) or (chen near3 sijian)) and ((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2)
5	(delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6
6	((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 program\$5
7	((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 program\$5) and (memory or memories or ram or dram or sram or fifo or (first adj in))
8	((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 program\$5) and (memory or memories or ram or dram or sram or fifo or (first adj in))) and modulator and order
9	((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 program\$5) and (memory or memories or ram or dram or sram or fifo or (first adj in))) and modulator and order) and register and delay\$4

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10	(((((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 program\$5) and (memory or memories or ram or dram or sram or fifo or (first adj in))) and modulator and order) and register and delay\$4) and (ic chip integrated adj circuit)
11	(((((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 program\$5) and (memory or memories or ram or dram or sram or fifo or (first adj in))) and modulator and order) and register and delay\$4) and (ic chip integrated adj circuit)) and port
12	(((((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 program\$5) and (memory or memories or ram or dram or sram or fifo or (first adj in))) and modulator and order) and register and delay\$4) and (ic chip integrated adj circuit)) and multiplier
13	(((((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 program\$5) and (memory or memories or ram or dram or sram or fifo or (first adj in))) and modulator and order) and register and delay\$4) and (ic chip integrated adj circuit)) and port and multiplier
14	((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 (program\$5 algorithm\$2)

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15	((((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 (program\$5 algorithm\$2)) and (memory or memories or ram or dram or sram or fifo or (first adj in)))
16	(((((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 (program\$5 algorithm\$2)) and (memory or memories or ram or dram or sram or fifo or (first adj in))) and modulator and order
17	((((((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 (program\$5 algorithm\$2)) and (memory or memories or ram or dram or sram or fifo or (first adj in))) and modulator and order) and register and delay\$4
18	((((((((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 (program\$5 algorithm\$2)) and (memory or memories or ram or dram or sram or fifo or (first adj in))) and modulator and order) and register and delay\$4) and (ic chip integrated adj circuit)
19	(((((((((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 (program\$5 algorithm\$2)) and (memory or memories or ram or dram or sram or fifo or (first adj in))) and modulator and order) and register and delay\$4) and (ic chip integrated adj circuit)) and port

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20	(((((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 (program\$5 algorithm\$2)) and (memory or memories or ram or dram or sram or fifo or (first adj in))) and modulator and order) and register and delay\$4) and (ic chip integrated adj circuit)) and multiplier
21	(((((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 (program\$5 algorithm\$2)) and (memory or memories or ram or dram or sram or fifo or (first adj in))) and modulator and order) and register and delay\$4) and (ic chip integrated adj circuit)) and port and multiplier
22	(((((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 (program\$5 algorithm\$2)) and (memory or memories or ram or dram or sram or fifo or (first adj in))) and modulator and order) and register and delay\$4) and (ic chip integrated adj circuit)) and port and multiplier) and programmable and algorithm
23	(((((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 (program\$5 algorithm\$2)) and (memory or memories or ram or dram or sram or fifo or (first adj in))) and modulator and order) and register and delay\$4) and (ic chip integrated adj circuit)) and port and multiplier) and pipelin\$4 and sequencer

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24	(((((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 (program\$5 algorithm\$2)) and (memory or memories or ram or dram or sram or fifo or (first adj in))) and modulator and order) and register and delay\$4) and (ic chip integrated adj circuit)) and port and multiplier) and delta near5 sigma near5 modulator
25	(((((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 (program\$5 algorithm\$2)) and (memory or memories or ram or dram or sram or fifo or (first adj in))) and modulator and order) and register and delay\$4) and (ic chip integrated adj circuit)) and port and multiplier) and delta near5 sigma near5 modulator) and (order same decimat\$3 same filter)
26	(((((delta-sigma or delta adj sigma or (delta and sigma)) and algorithm\$2 and program\$6) and (select\$4 different variable chang\$4 adjust\$5) near6 (program\$5 algorithm\$2)) and (memory or memories or ram or dram or sram or fifo or (first adj in))) and modulator and order) and register and delay\$4) and (ic chip integrated adj circuit)) and port and multiplier) and delta near5 sigma near5 modulator) and (order same decimat\$3 same filter) and register adj file and pipelin\$4 and shift adj register and add\$4 and coefficient and delay\$4
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28	5345409.pn.

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